Integration of AGATA electronics: first results

- Week 21, May 19-22
  - First traces from AGATA digitiser reach Carrier
    P.J. Coleman Smith, X.Lafay, Padova Team
- Week 22, 23, May 26-30, June 3-6
  - Problem of broken traces solved
    Padova Team
- Week July 1-5
  - First online data and spectra from S001 detector
    X.Lafay, Padova Team

Padova Team = M. Bellato + D.Bortolato + R.Isocrate + J.Chavas + A.Triossi

Dino Bazzacco

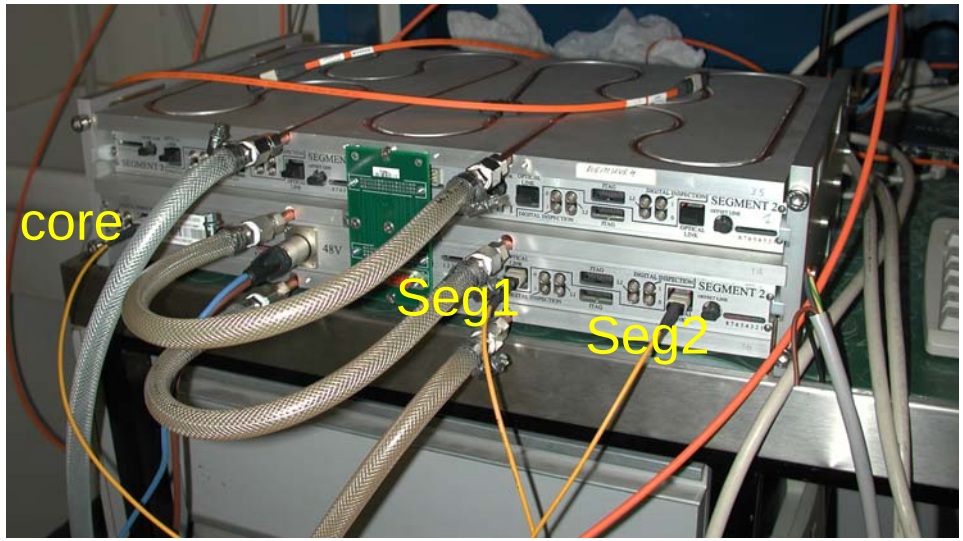
Goal is to take data from an AGATA detector using AGATA electronics before the end of July 2008

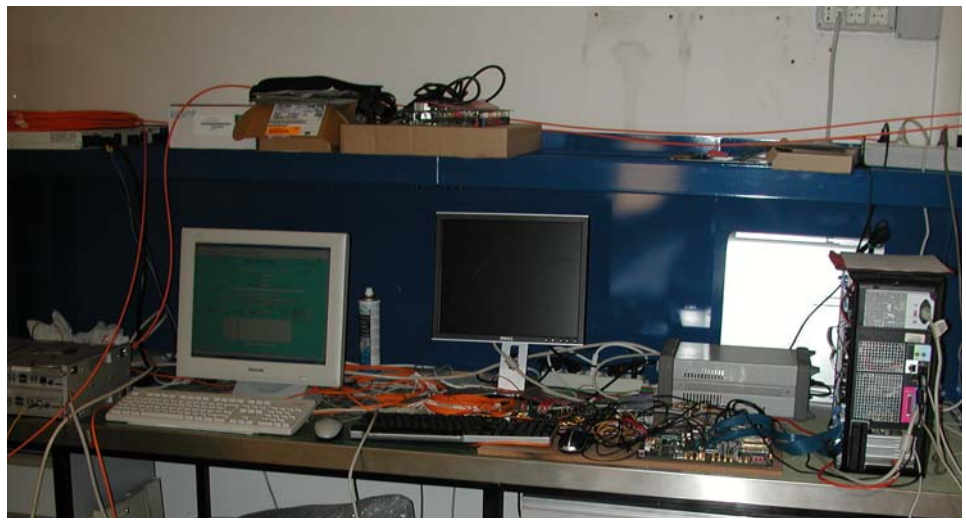
- ✓ Detector with its 36 segments and 1(2) core
- ✓ Digitiser operated in “sample and transmit” mode with external clock provided by the GTS system
- ✓ Serial transmission of the digitized samples to the pre-processing electronics located 75 m (of optical fibre) away
- ✓ Read-in and de-serialization of the bit stream from the fibre
- ❖ Generation of local trigger in the core mezzanine
- ➢ Energy analysis and trace capture in the pre-processing mezzanines (core and segments)
- ➢ Readout (PCIe) to ACQ PC of GTS-validated events

Detector → Digitiser → 75 m optical fibre →

→ Segment Mezzanine → Local processing → ATCA carrier → PCIe → PC

Equipment on the detector side





-S001 detector with dual core preamp.
-Pulser fed to “detector emulator” GPBox[1]
-AGATA digitiser from series production
-Control computer[2] and the snapshot system[3]

1-George Pascovici 2-Vic Pucknell 3-Patrick J. Coleman Smith

Equipment on the pre-processing side

ATCA Carrier
Trigger receiver
Segment mezzanine (2)
GTS mezzanine
Control computer
Data Acquisition computer

Damiano	Bortolato
Marco	Bellato
Xavier	Lafay
Andrea	Triossi

❖ Surviving without core mezzanine

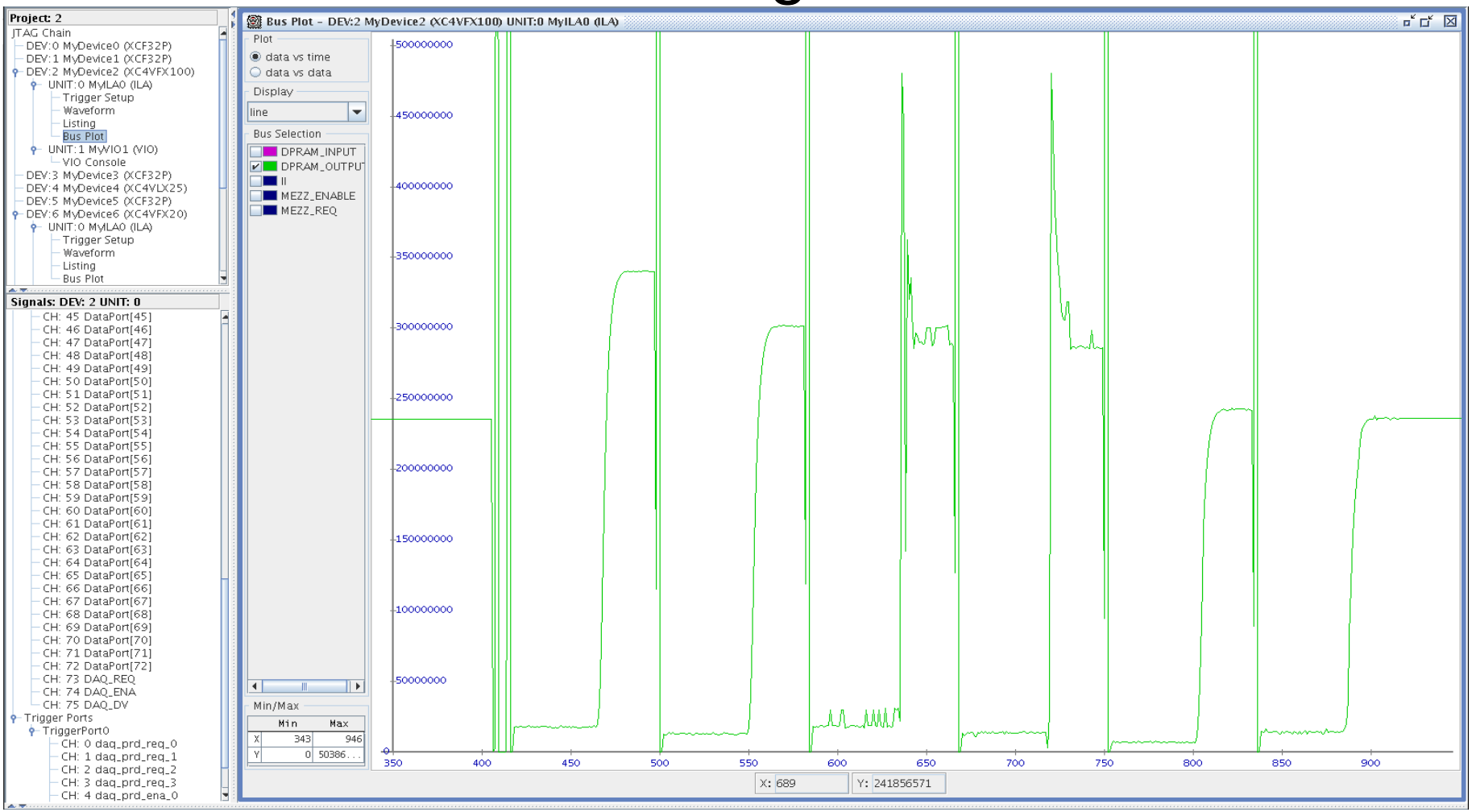
- Clock and Sync pulses provided to the digitiser directly by the GTS mezzanine
- Trigger generated externally* (CGD, rate-meter of a spectroscopy amplifier or, from local trigger in digitiser when implemented) and injected to GTS by means of a “pseudo core”
- Output of core digitiser put to one channel of a segment mezzanine by means of splitter-cables

*for the final spectra, the trigger signal was taken from 2nd channel of the dual core preamplifier by soldering wires to the + and ground pins (patch by Daniele…)

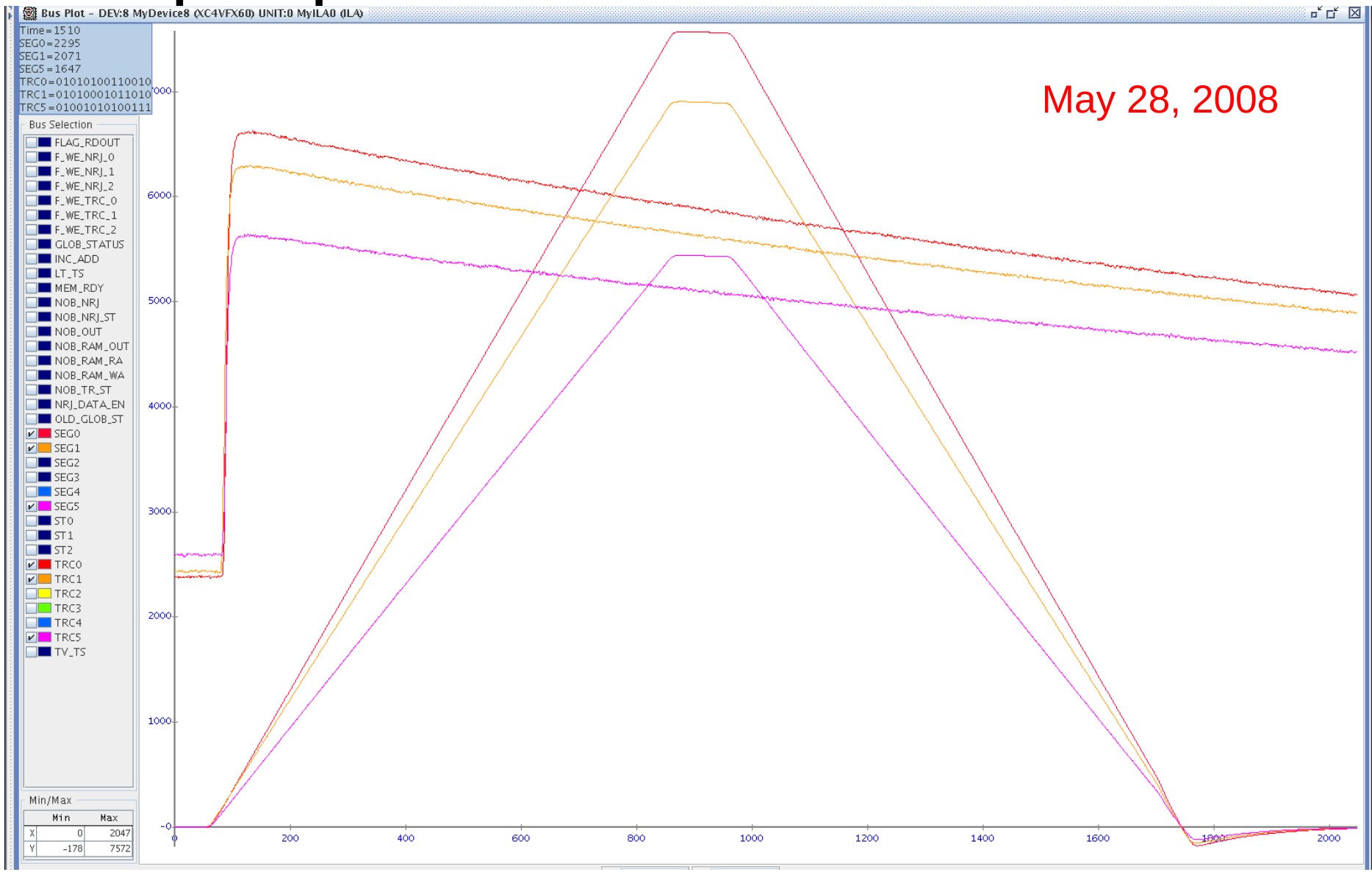
May 22, 2008,

THE FIRST AGATA TRACE

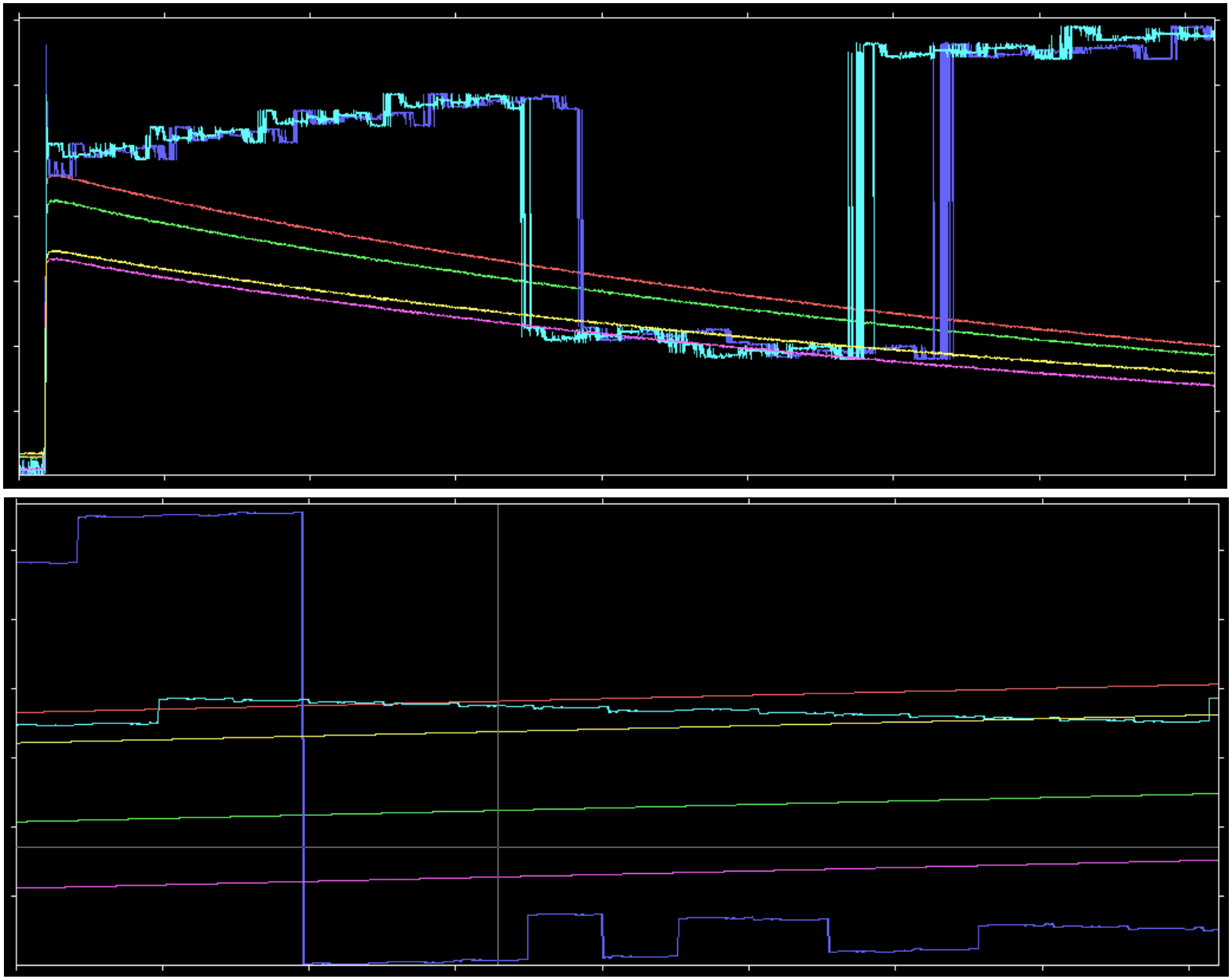
makes its way from the digitiser to the ATCA-carrier, via segment mezzanine.



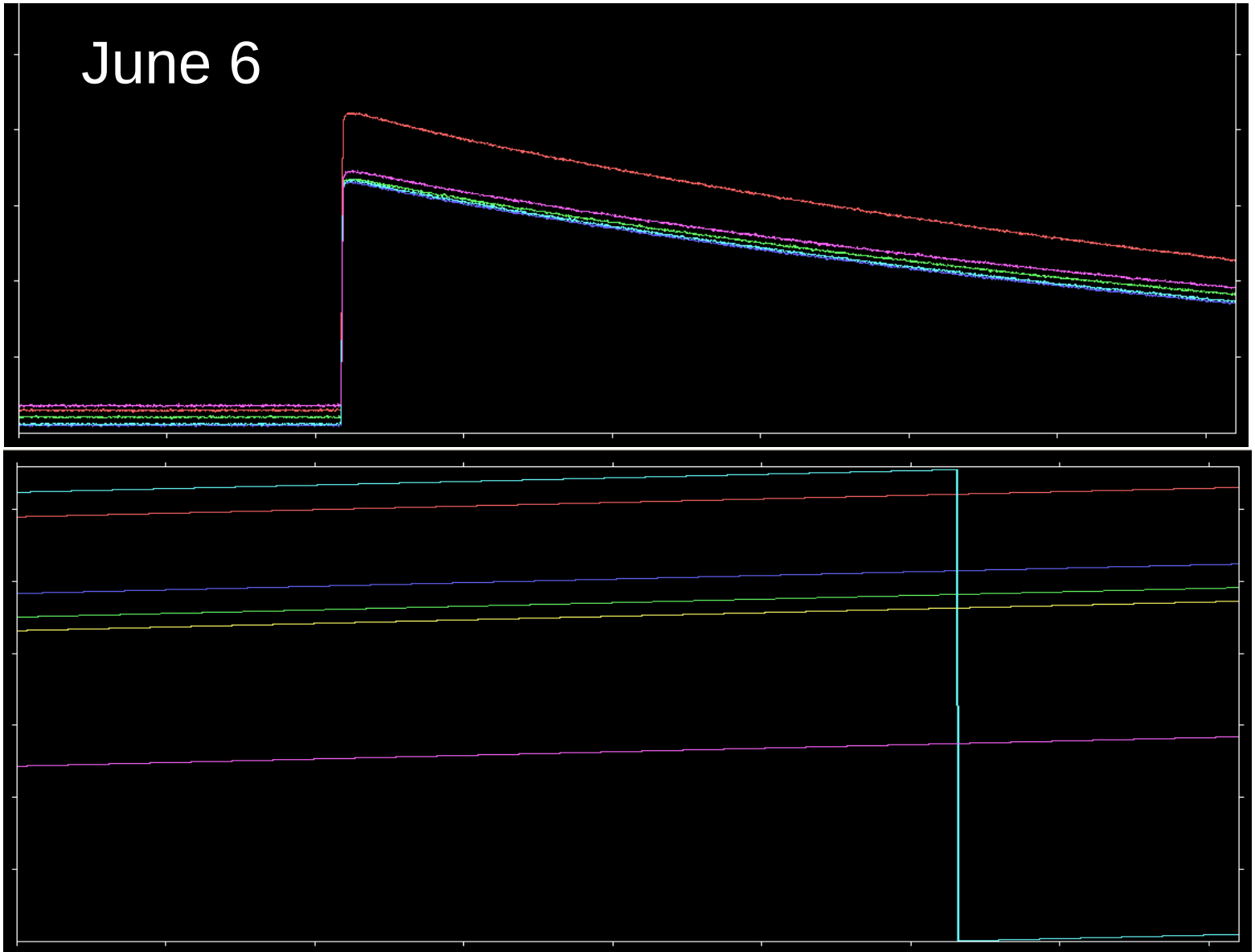
Digitized, optically-transmitted and pre-processed AGATA traces



Pulser and Ramp by end May

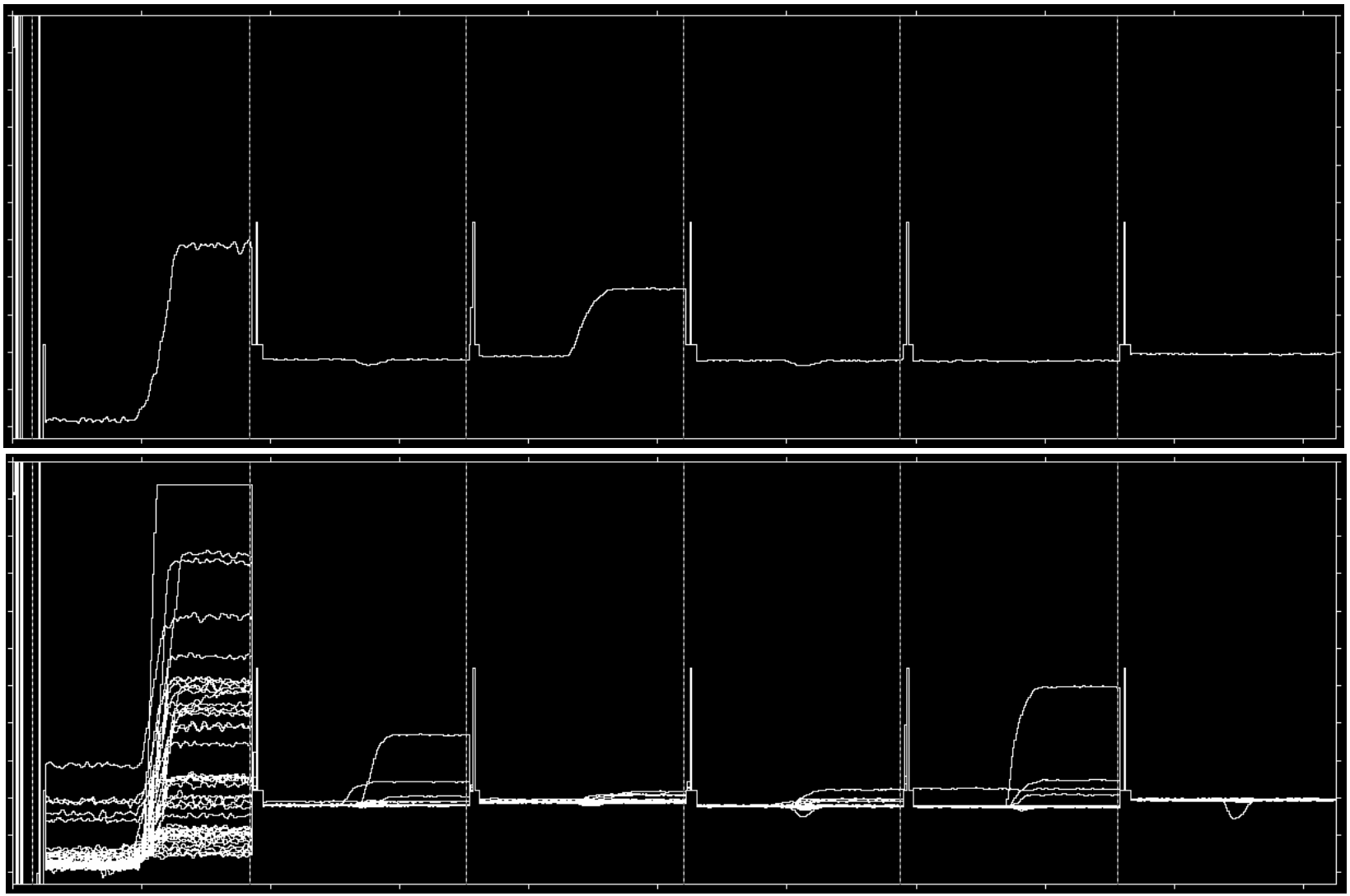


Pulser and Ramp after fixing polarity inversion problem



First events readout via PCIe July 4

Readout speed > 100 Mb/s, limited by disk access



Provisional data format from PP

Item		Length in 16-bit words
Mezzanine header		16
Channel 1	header	8
	trace	160 samples
Channel 2	header	8
	trace	160 samples
Channel 3 … 6		

0	Mezzanine ID
1	Event number (2 words)
2	
3, 4, 5	Timestamp (3)
6	Number of samples in trace
7…15	Spare

0	Channel ID
1, 2	Energy 2 words (need to modify MWD)
3	Channel status (pileup, over/underflow…)
4… 7	Spare (e.g. BL value, energy from ToT …)

Length of Segment mezzanine block
→ 16+6*(8+160) = 1024 words

Length of Core Mezzanine block
→ 16+2*(8+160) = 352 words

Length of event from Carrier 0 (CC+2 SG)
→ 352 + 2 * 1024 = 2400 words
(430 events in the 2 MB of DPRAM)

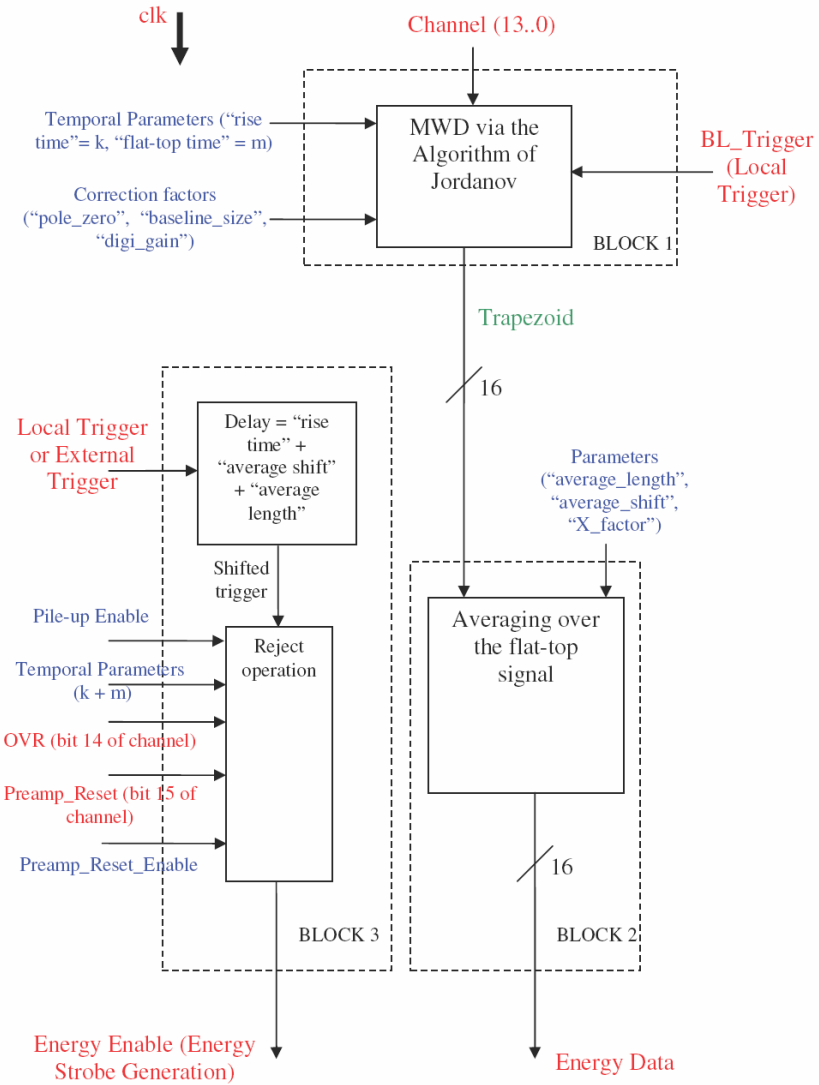
Length of event from Carrier 1 (4 SG)
→ 4 * 1024 = 4096 words
(256 events in the 2 MB of DPRAM)

Total length of event → 6496 words

Possibility to reduce length by ~50 %

Energy Block for the Mezzanine card

Provided as a net-list by IPHC Strasbourg (Laurent Charles)
Integrated into the SegMezz FPGA by CSNSM (Xavier Lafay)



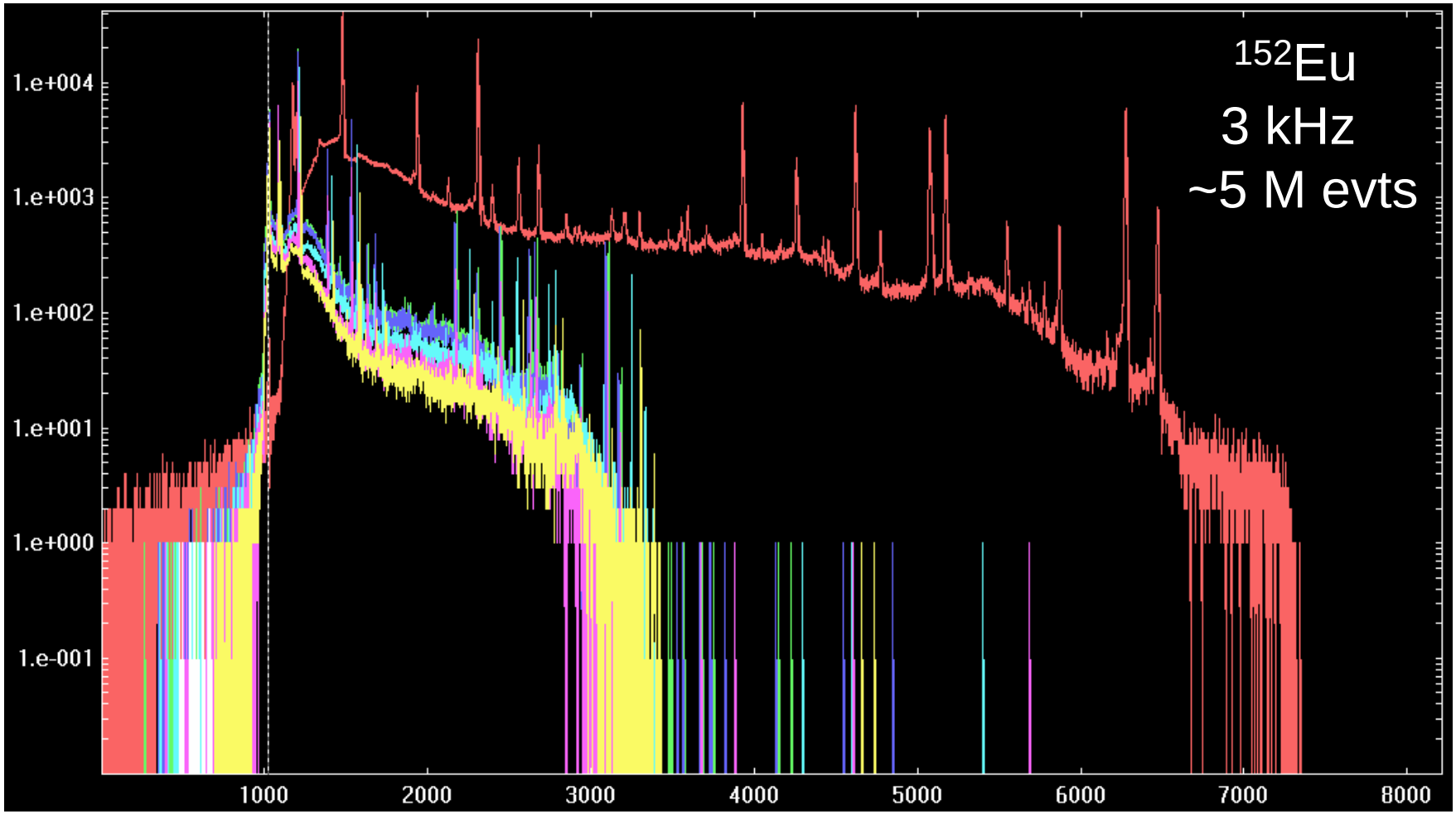
Integration was more difficult than expected as slow control still missing → every change of parameter implied recompiling the whole project (~30 m)

Real progress done on Saturday, July 5, when Damiano implemented control of parameters I2C in bus

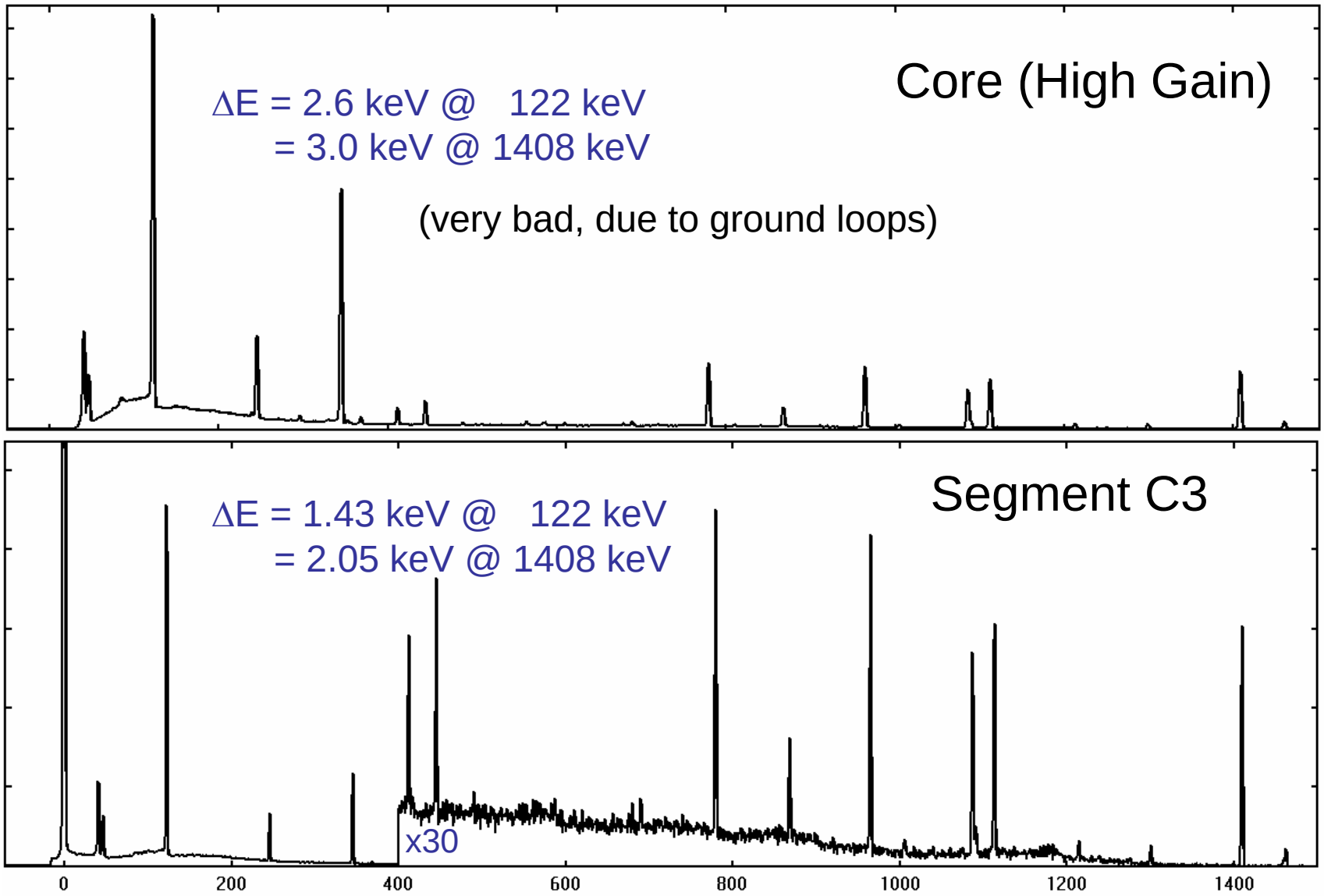
Problems and Improvements

- digital_gain does not work properly (?)
- write-out energy with 32 bits
- remove energy averaging block (?)
- remove reject operation block !
- automatic threshold of base line restorer !
- deconvolution of multiple poles (?)

“Stable” operation reached on Saturday, July 5, late afternoon



Energy resolution



Major problems to solve

- Only Damiano is able to run the system → ???
- Start/Reset procedure not fully understood → ???
- Not all local triggers produce a readout → pipelined architecture
  - Retriggering before trace capture
  - Retriggering before energy capture on flattop
  - Retriggering before end of trapezoid ?
  - Retriggering while readout blocked is ignored
- Base line restorer taken from local trigger → automatic blr

Simpler ToDo's

- Add an absolute identifiers to the label of mezzanine frames
- Minimize latency used to compensate MGT differences
- Fix ordering of words in PCIe readout
- Modify energy block to write-out energy with 32 bits

More general issues

- Integration requires lots of manpower concentrated at the integration site
- How to manage core till arrival of core mezzanine
- Implementation of ToT
- Deconvolution of multiple poles
- Removal of offset from input traces to ease PSA → deconvolution of traces